GOVERNMENT ENGINEERING COLLEGE – DAHOD

IIC, GIC & SSIP 2.0 CELL

REPORT

One day workshop on
"Innovations with VLSI: Exploring Circuit Design with EDA Tools"

The one-day workshop on **"Innovations with VLSI: Exploring Circuit Design with EDA Tools"** was successfully organized on 3rd November, 2023, for the students of ECE department of Government Engineering College Dahod. The workshop was held at ECE dept, GEC Dahod. The event was held under the collaborative efforts of IIC & GIC, and SSIP 2.0 Cell, showcasing the commitment to fostering innovation and knowledge-sharing in the field of VLSI. Total 26 students from the 3rd, 5th and 7th semesters attended the workshop. Participation certificates were issued to all the attendees.

The event commenced with a warm welcome to the guests, including Guest Expert **Prof. N.K.Patel Assistant professor at GEC Godhara, Principal (in-charge) Dr. P. B. Tailor, IIC&GIC President Dr. D. B. Jani, and SSIP 2.0 Cell President Dr. M.K. Chudasama, Head of the ECE Dept Prof S.M.Vaishnav**. **Event coordinators, Prof A.B.Vaghela and N.K.Saini**, facilitated the guests with flowers, setting a positive tone for the workshop.

Detailed Scheduled of Workshop:

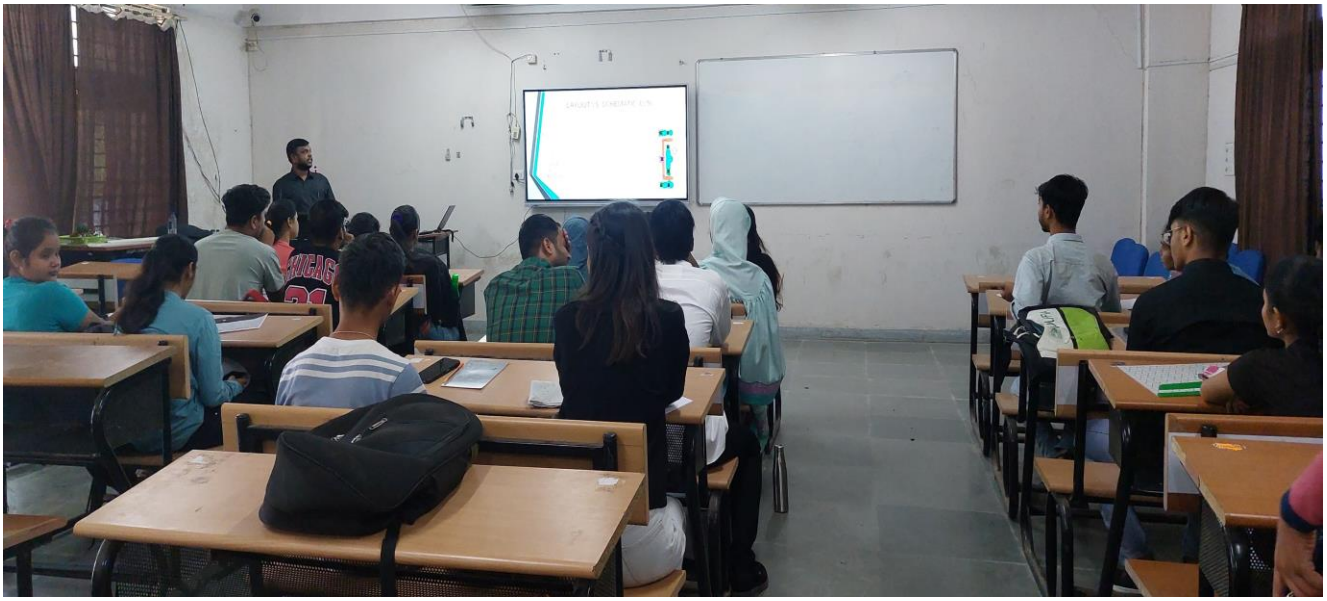
Time	Session / Topic
10:45 AM – 11:15 PM	Inauguration & Key Note Speech on Current Trends and Challenges of VLSI Design
11:15 AM – 12:30 PM	VLSI Design Flow (Speaker: Prof. N K Patel)
12:30 PM – 1:15 PM	**Lunch Break**
01:15 PM – 3:15 PM	Introduction To EDA Tool – Hands on Session Pre-layout simulation (Speaker: Prof. A B Vaghela)
03:15 PM – 3:30 PM	**Tea Break**
03:30PM – 05:15PM	Hands on Session Post-layout simulation (Speaker: Prof. N K Patel)
05:15 PM - 5:30PM	Valedictory

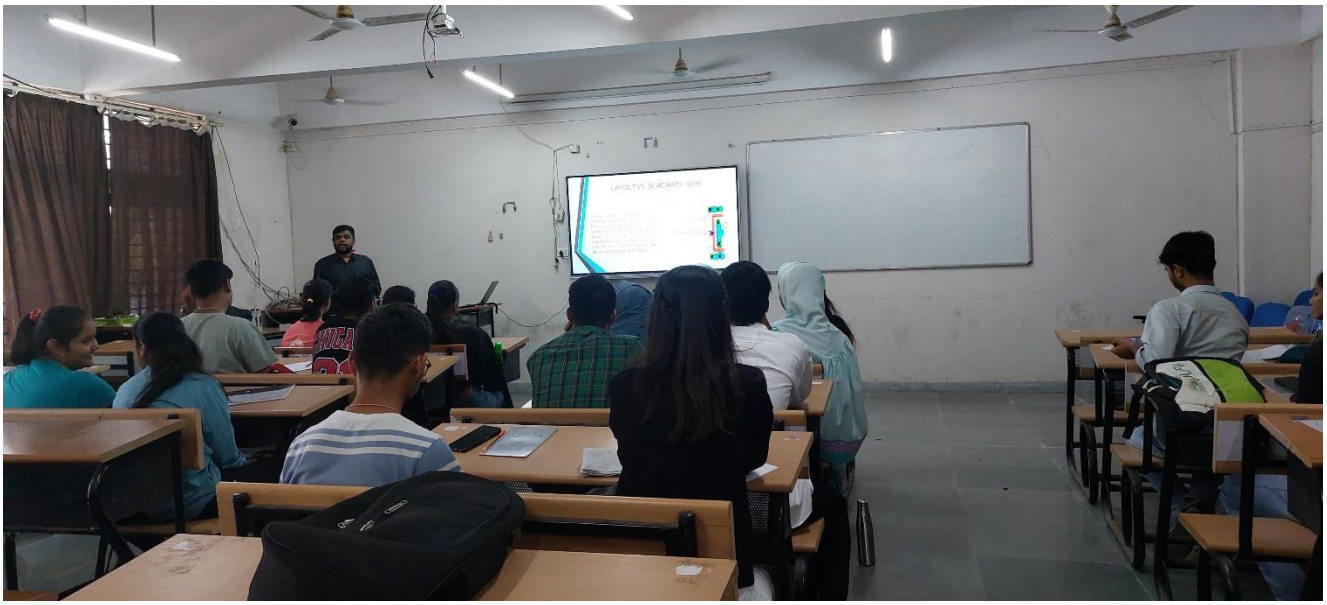
The workshop is divided into 3 sessions.

Morning Session (11.15am-12.30pm): Morning Session (11.15am-12.30pm) was held in seminar room at ECE Dept .GEC Dahod :Prof. N.K.Patel delivered a lecture on current trends and challenges in VLSI Design and explained various basic concepts of the CMOS Inverter and its application. Introduced EDA Tools, specifically highlighting Cadence software.
Afternoon Session (1.15pm-5.15pm): was held in Computer Lab at ECE Dept .GEC Dahod **On first half Session** (1.15pm-3.15pm): **Prof A.B.Vaghela** conducted a hands-on session using Cadence software of CMOS inverter and performed Pre-Layout simulation. **On second half Session** (3.30pm-5.15pm):**Prof. N.K.Patel** led a hands-on session using Cadence software and performed Post-Layout simulation of the CMOS inverter.
Valedictory Session: A memento of honor was presented to **Guest Expert Prof. N.K.Patel by the Head of the ECE Dept. Prof A.B.Vaghela** delivered a vote of thanks.

Photos of Workshop


GOVERNMENT ENGINEERING COLLEGE – DAHOD
EC DEPARTMENT
EC DEPARTMENT
Organized a
One Day Workshop
Under
IIC, GIC & SSIP 2.0 CELL



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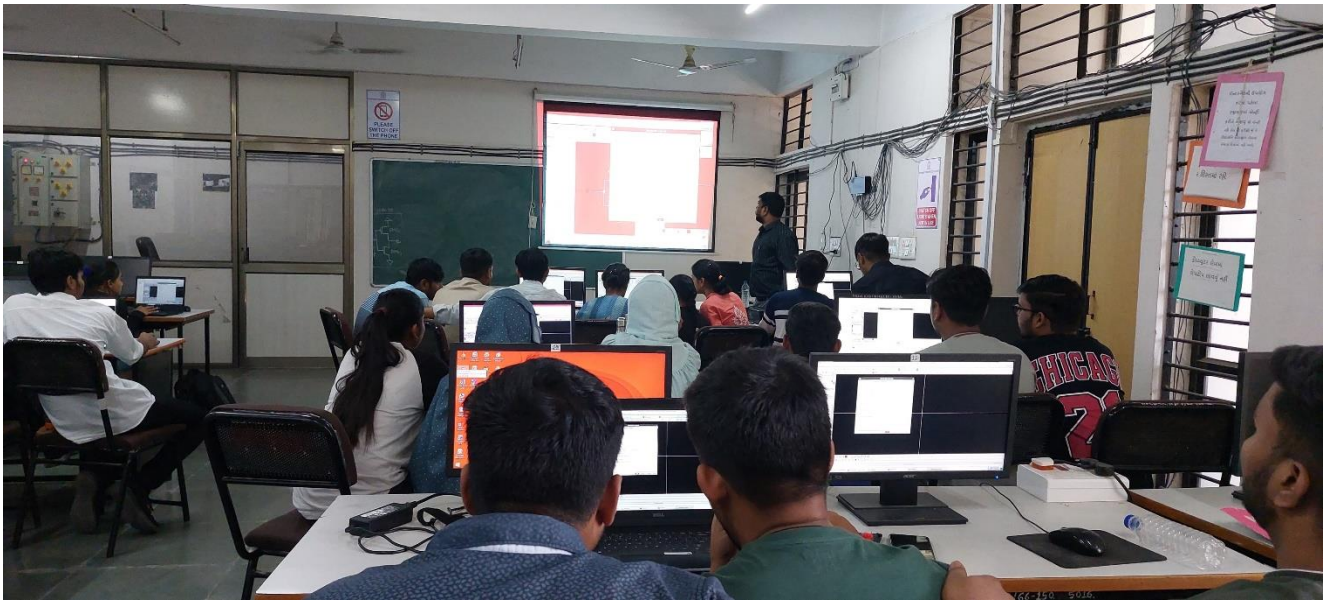

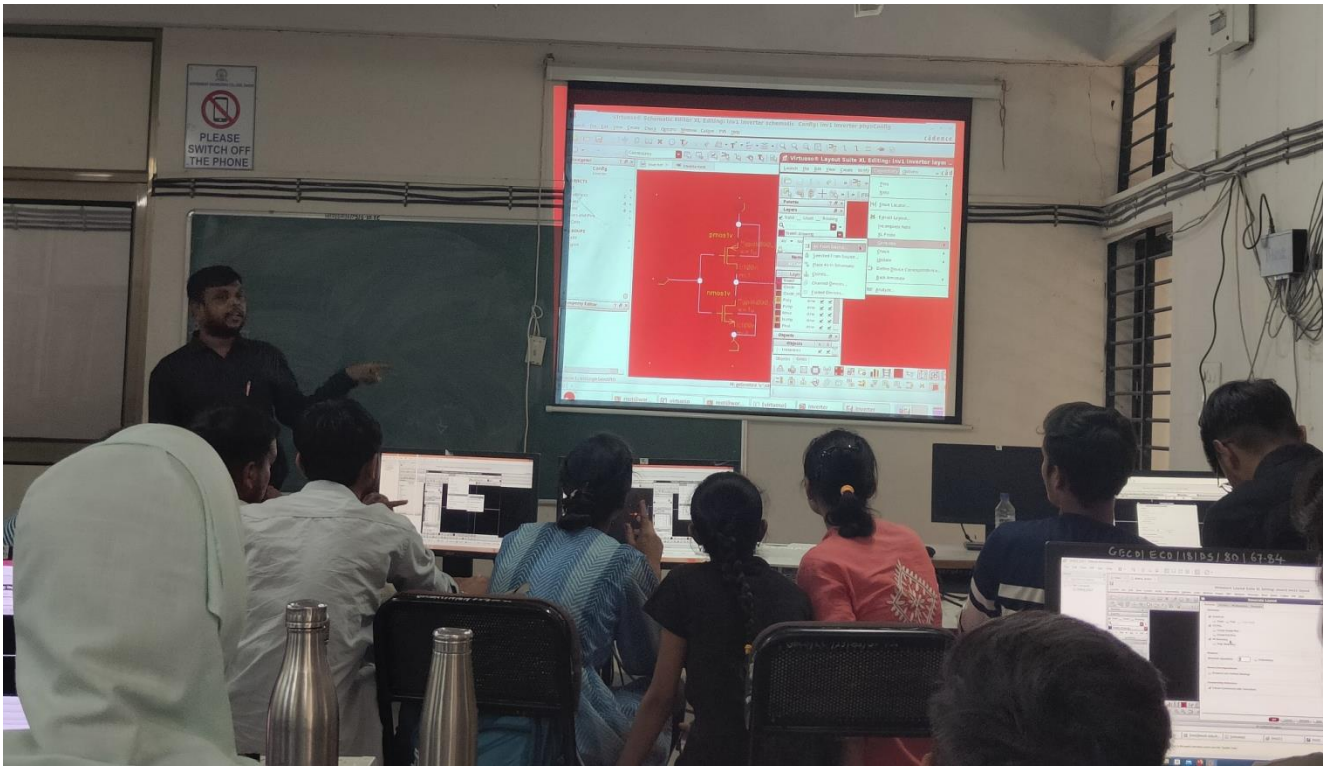
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